CMS pixel detector upgrade

Valeria Radicci

University of Kansas

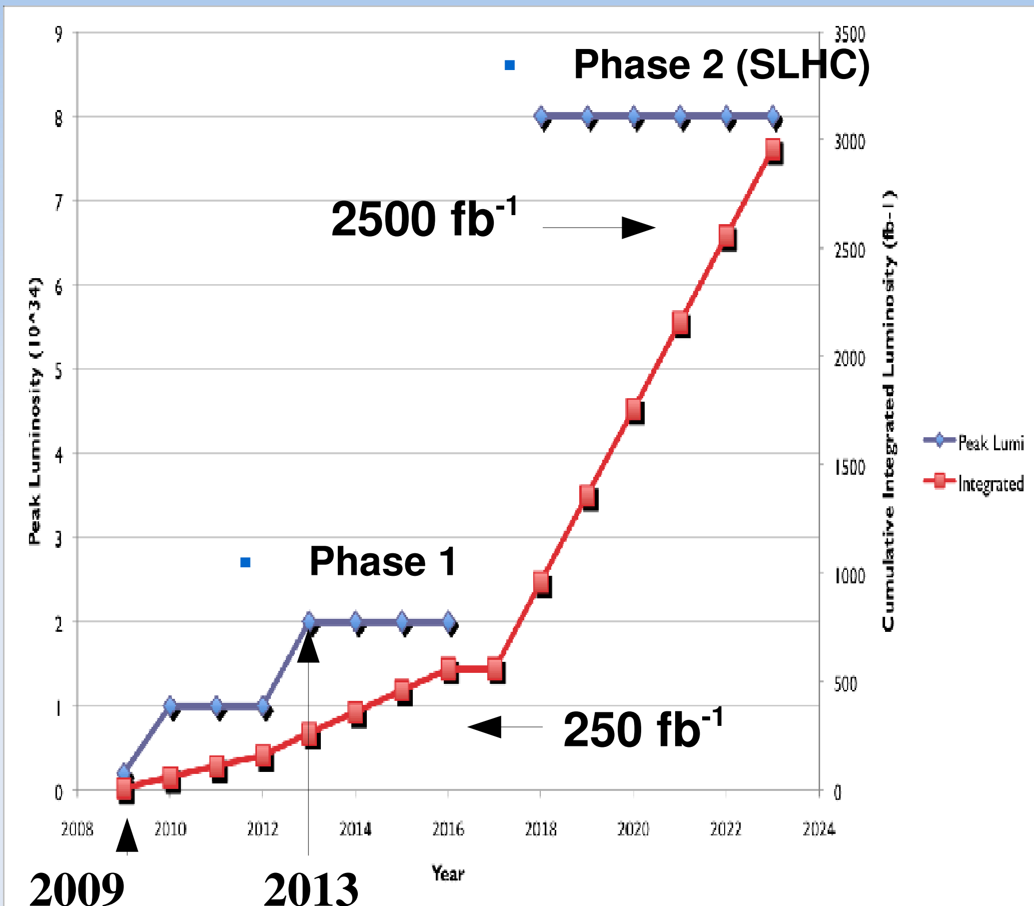
- LHC machine upgrade and implications for the CMS tracking system
- Inefficiencies of the present CMS pixel detector for LHC ugrade
- Status of the R&D activities at PSI
- Possible scenarios for the intermediate detector upgrade
- Conclusions

Motivation for an LHC Luminosity Upgrade

- LHC accelerator will provide p-p interactions at an energy of 14TeV and a peak luminosity of 10^{34} cm^{-2} s^{-1}, ~ 100 fb^{-1}/year.
- after a few of years of running at design luminosity whatever new physics is observed, its understanding will require higher statistics and higher energies.
- LHC upgrade is foreseen
- No other facility in the world can achieve this in a foreseeable future.

European Strategy for Particle Physics:
"... A subsequent major luminosity up-grade (SLHC), motivated by physics results and operation experience, will be enabled by focused R&D; to this end, <u>R&D for machine and detectors has to be vigorously pursued now and centrally organized towards a luminosity up-grade by around 2015.</u>"

LHC Luminosisty Upgrade plan



J. Nash - CMS Ugrades CERN 21 May 2008

Nominal Peak Luminosity:

- **2009 → 2013**
  $L_{PEAK} = 1x10^{34}\ cm^{-2}\ s^{-1}$
- **Phase 1 (Intermediate upgrade)**
  $L_{PEAK} = 2x10^{34}\ cm^{-2}\ s^{-1}$
- **Phase 2 (SLHC)**
  $L_{PEAK} = 8x10^{34}\ cm^{-2}\ s^{-1}$

Beam luminosity →

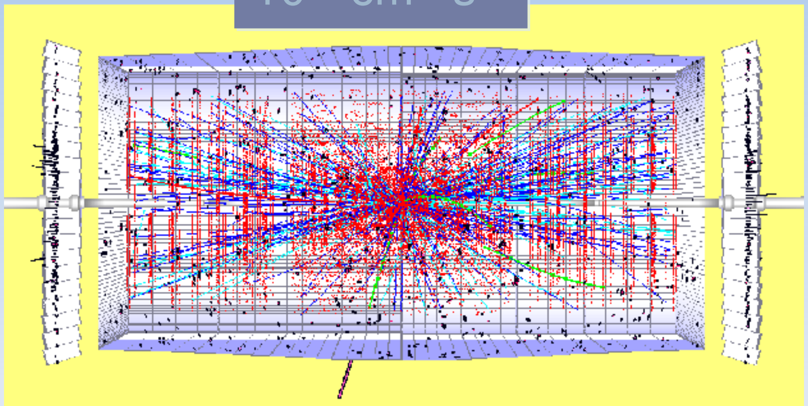
→ Occupancy of the read out electronics

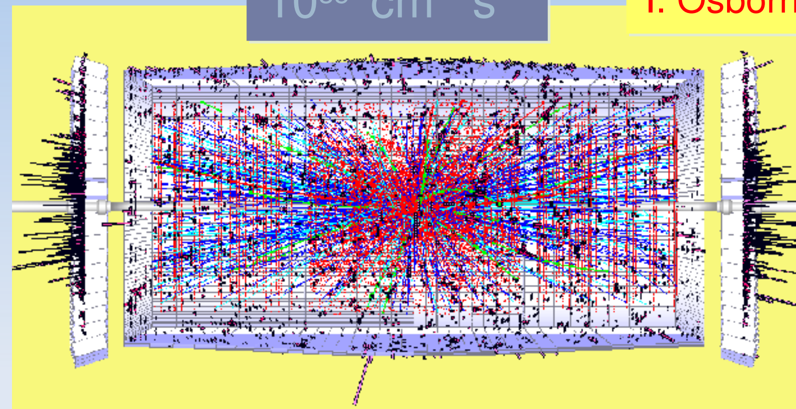
→ Radiation damage of the components

LHC detectors were not defined for SLHC luminosity!

LHC Luminosisty Upgrade plan

LHC → **SLHC**

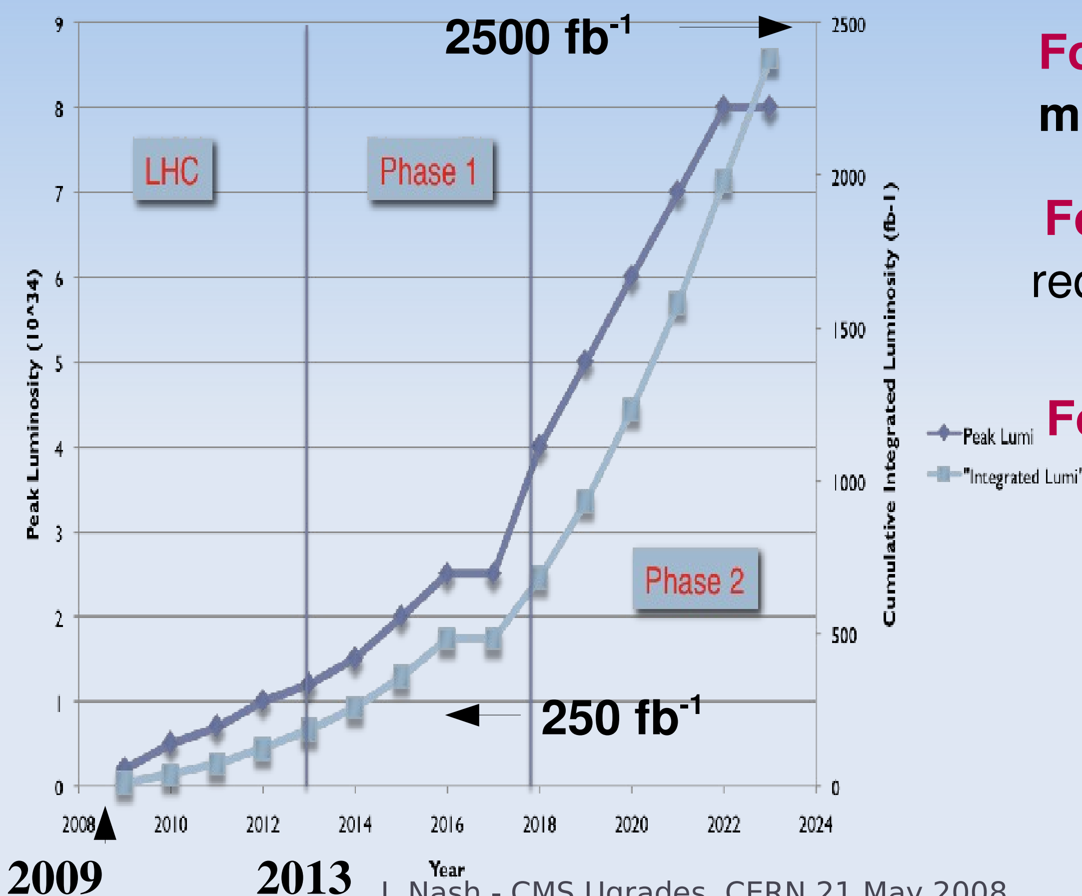




I. Osborne

	LHC	SLHC
Full luminosity	LHC ~20 interactions/bx	SLHC 300-400 interactions/bx
Occupancy (read out electronic)	**Inner pixel layer:** already close to the limit (i.e. data loss ~4%)	**Inner pixel layer:** new readout chip
Radiation damage on sensors	**Inner pixel layer:** needs replacement every two years	**Tracker:** will become inefficient. New design!

A more realistic scenario



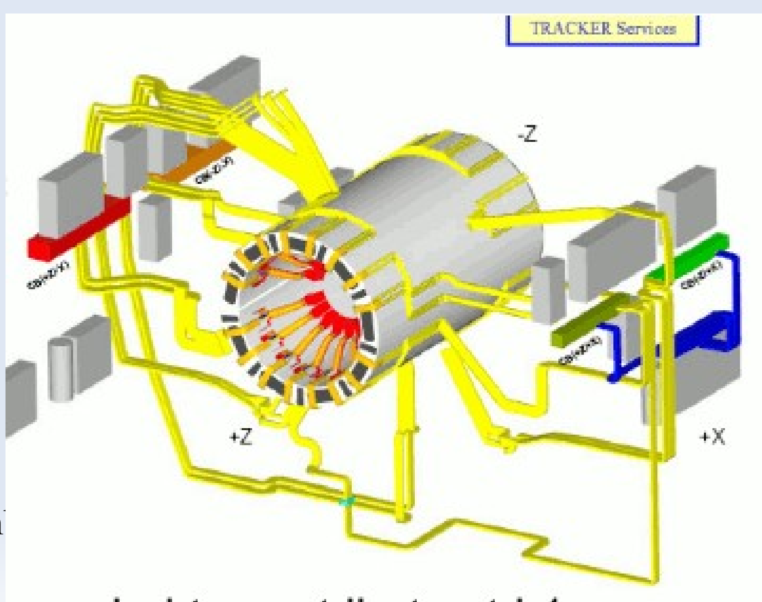
J. Nash - CMS Ugrades CERN 21 May 2008

For Phase 1: replace the sensors and may upgrade the chip

For Phase 2: the **whole pixel** detector will require **upgrading**

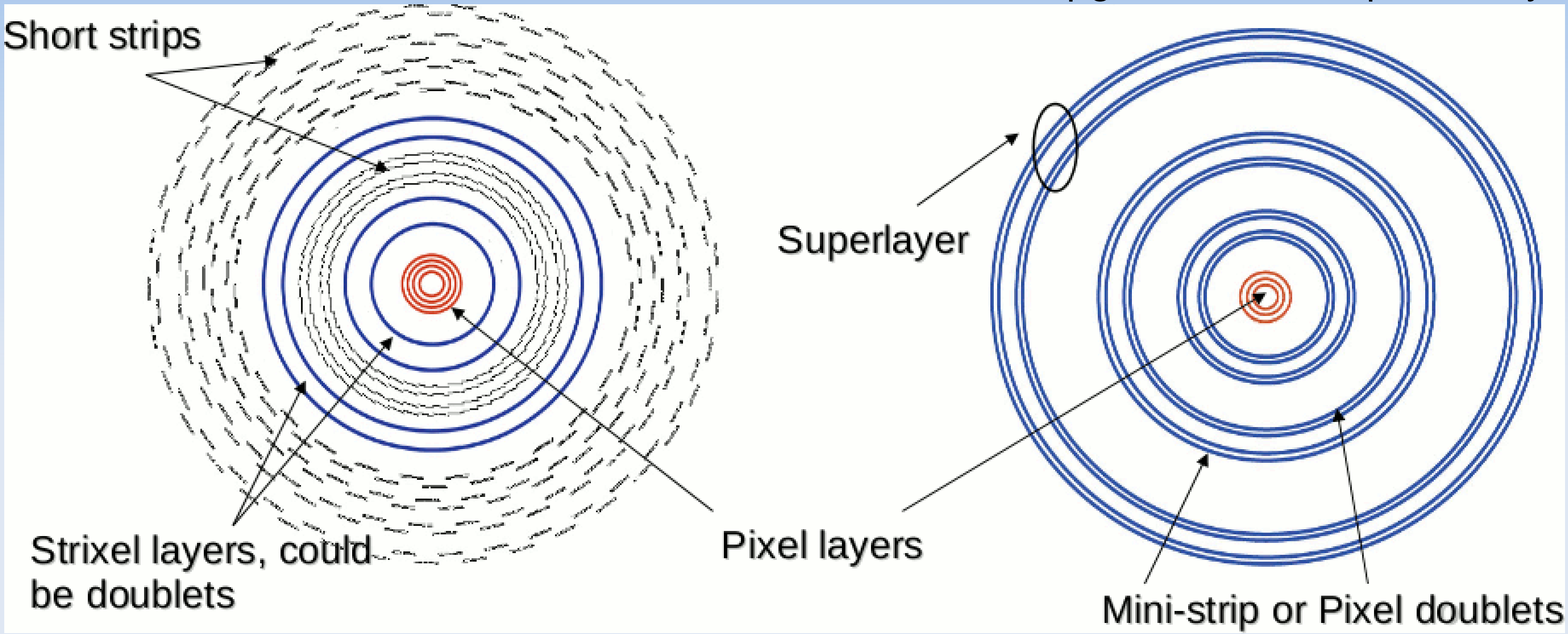
For both Phases boundary conditions:

- achieve similar performance
- no increase (ev. reduce) the material budget
- all existing services must be reused (cables, fibres, cooling)



Tracker barrel strawman designs for Phase 2

A. Tricomi CMS SLHC Upgrade Workshop, 21 May, 2008



Strawman A Geometry:

Perturbation of current tracking system

4 Inner pixel layers, 2 strixel + 2 short strip layers (TIB), 2-strixel + 4 short strip layers (TOB)

Strixel 1,2 (TIB) 100µm x 600µm strixel size

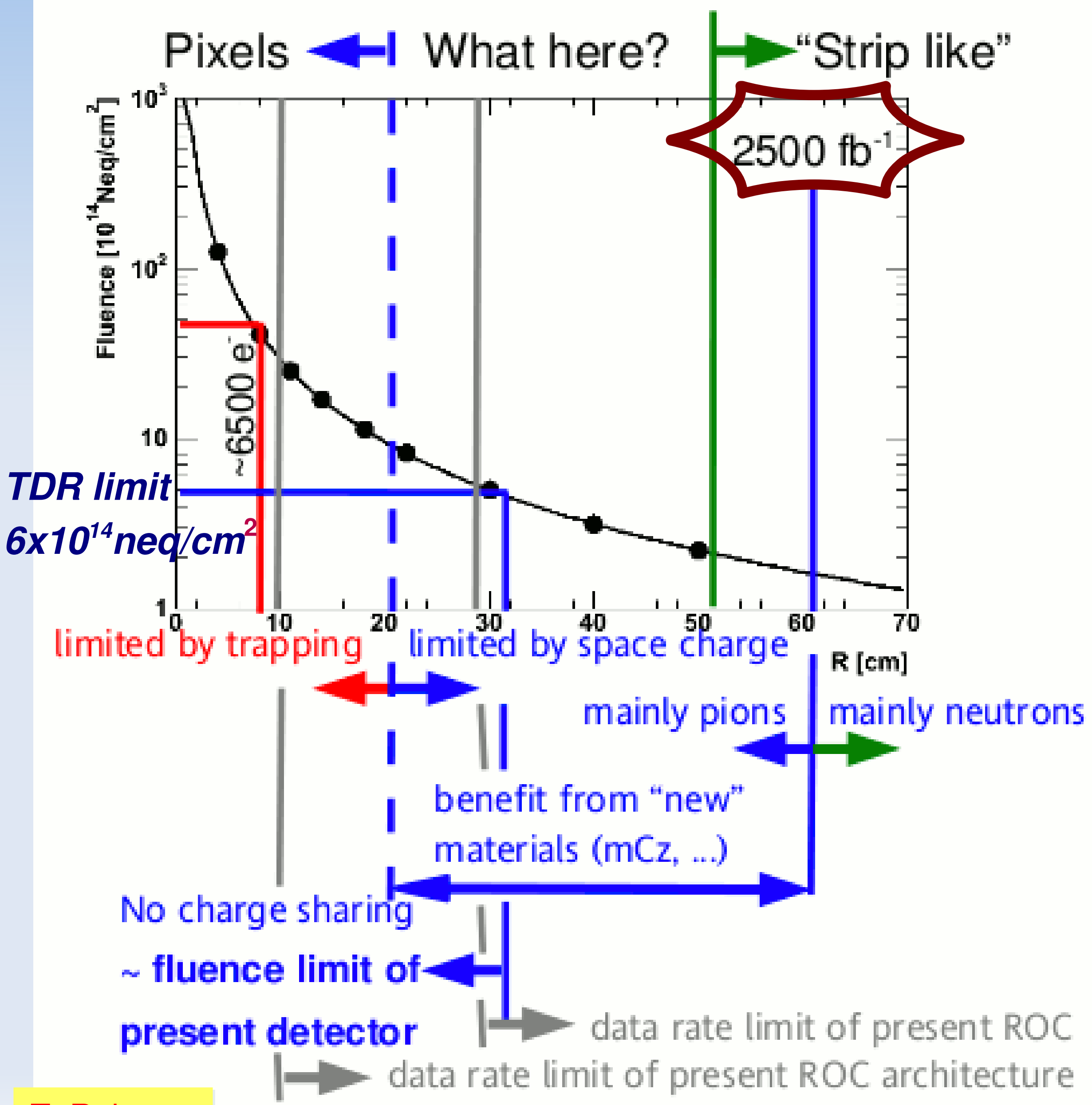
Strixel 3,4 (TOB) 100µm x 1200µm strixel size

Strawman B Geometry:

Design radically different from current tracker:

3 Inner Pixel layers, Short strips Super-layers, each with two doublet layers (integrated tracking/ triggering layers);

Silicon Sensor Limitations



r > 50 cm:

- **mainly neutrons:**
  - Cheap p+ on n

20cm < r < 50 cm:

- performance **limited by space charge:**
  - **Collect e-** (n+/n or n+/p)
  - CAN be improved by **MCz, DOFZ** material.

8cm < r < 20 cm:

- performance **limited by trapping:**
  - **Collect e-** (n+/n or n+/p)
  - NOT improved by material (Mcz, DOFZ...)

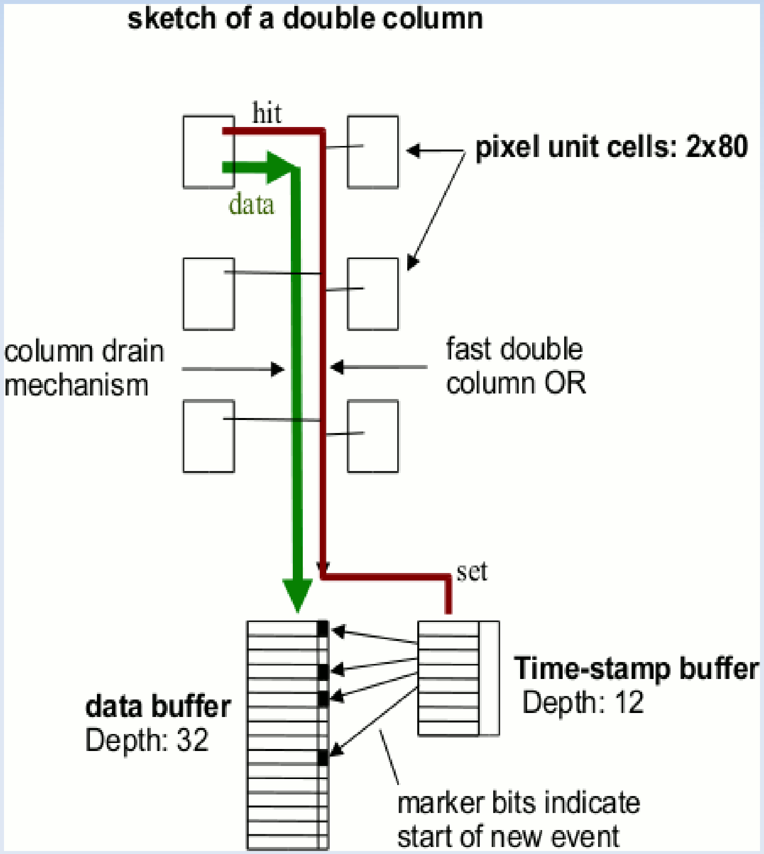
4cm < r < 8 cm:

- Present **limit of readout** 6000e- (new chip design)
- frequent replacement or new solutions.

T. Rohe

Data loss mechanism

High rate tests and simulation of the Pixel ROC have shown inefficiency of the data transfer mainly due to *buffer limitation* and the *dead time* of the ROC read out while transferring data to the TBM.



For Luminosity: 1 x 10^{34} $cm^{-2}sec^{-1}$

Radii = 11 cm / 7 cm / 4 cm layer

Total data loss @ L1A =100kHz

- **0.8%**
- **1.2%**
- **3.8%**

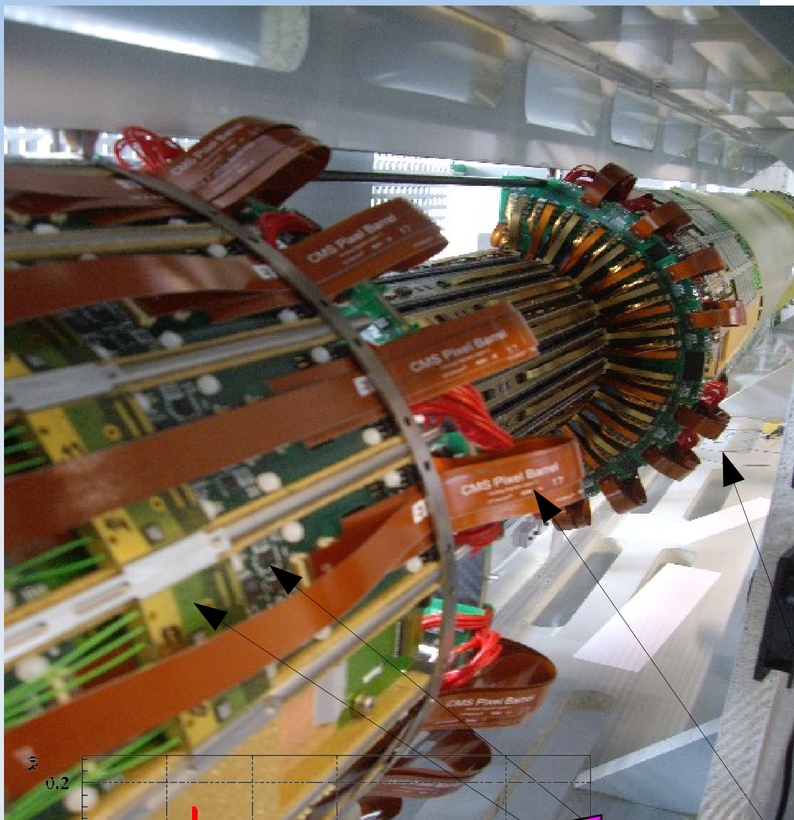
This is suitable for LHC, improvements needed for inner layers for SLHC

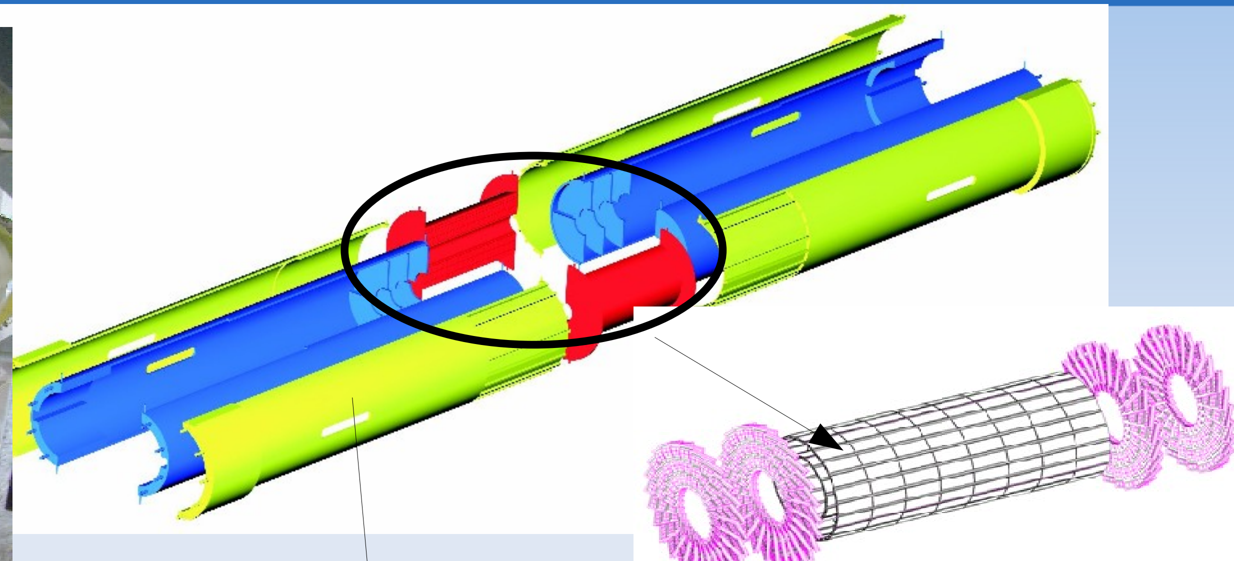
Possible solutions:

- **Doubling the buffer size**
- and/or redesign TBM for **parallel ROC readout**

- (R. Horisberger, SLHC meeting at CERN 21/05/08)

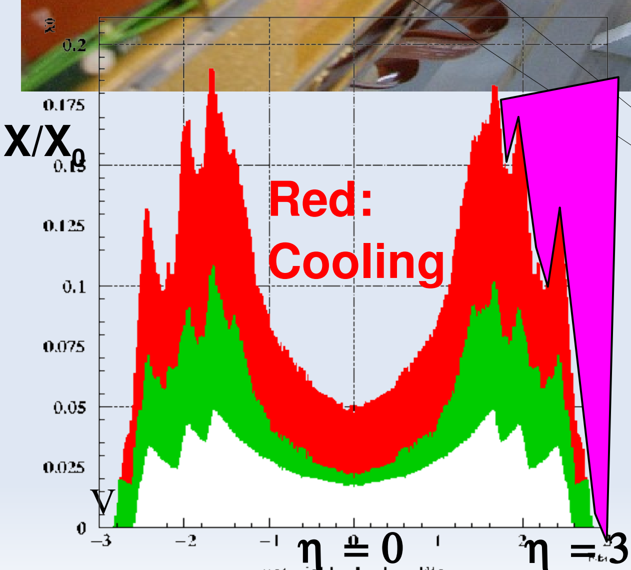
Material budget contributions



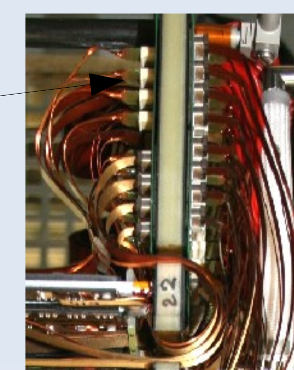


White: Barrel and Forward

- Silicon sensors
- C-fibre mechanical structure
- Cooling pipes



- **Magenta: Supply tube**
- Very complex, expensive PCB endflange prints with ~800 plugs!
- High density kapton signal cables
- DOH - AOH + PCB mother board

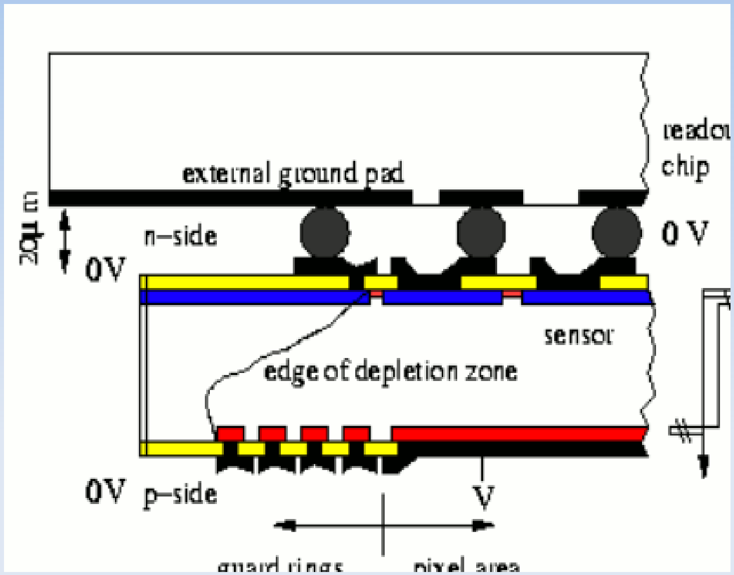


Green: Electrics

Sensor R&D for High Doses

Actual CMS Barrel Pixel Sensor design:

- n+ on n substrate
- 150x100µm pixel
- distance between pixel implants 20µm (Gap)
- DOFZ (standard FZ material enriched with oxygen on wafer)
- inter-pixel isolation moderated p spray
- bef. irra. junction and guard ring on back side
- aft. inversion junction on the pixel side

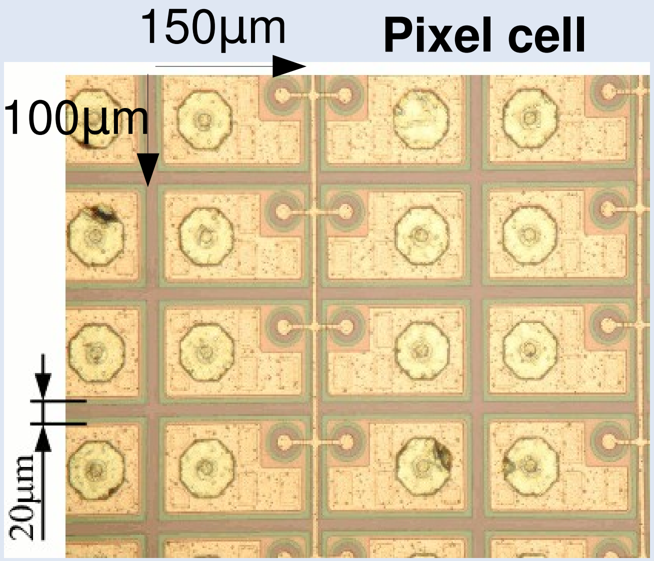


R&D plan:

(I) try to determine the ultimate limit of the **detection efficiency and loss of the signal charge by trapping**

(II) Investigate slightly modified sensor geometry (Gap = 20, 30µm) with **capaitance measurements**

(III) Characterization of n+ on p, DOFz and Mcz before and after irradiation.



Sensor R&D for High Doses

Last irradiation campaign of CMS barrel pixel sensor during 2007:

- 24GeV protons at CERN
  - 4 fluences up to 5.1×10^{15} neq/cm^2
  - 33 samples (Gap20 and Gap30)
- 300MeV pions at PSI
  - 3 fluences up to 6.2×10^{14} neq/cm^2
  - 14 samples (Gap20 and Gap30)

Charge Collection Efficiency Measurement:

Sr90 source

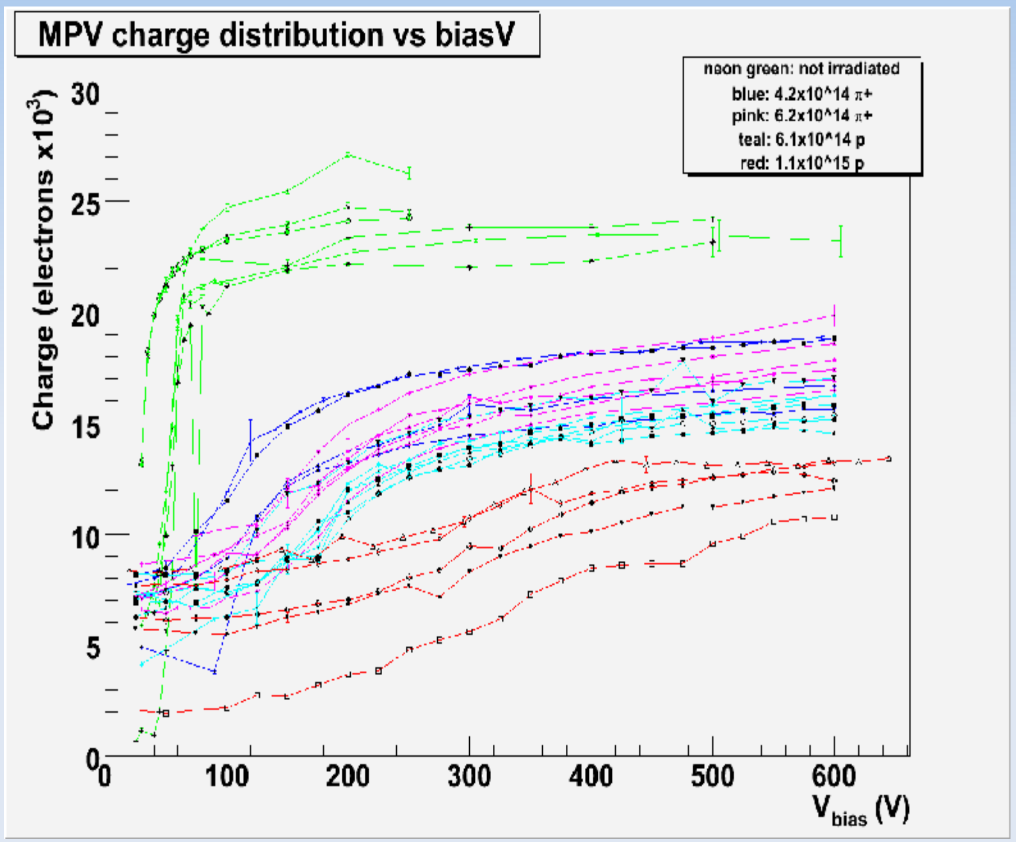
Cold box ~-10^{0}C

CCE Set Up @ PSI

PIRE students at PSI and T. Rohe

Sensor R&D for High Doses

- ROC calibration and charge measurement without any problem **up to 1.1×10^{15} neq/cm^2**
- @ 1.1×10^{15} neq/cm^2 @ T=10^0C
  - **Charge > 10000 e^- (CCE~50%)**
  - **V_{dep} ~ 450V**
- @ the last two fluences the calibration of the ROC settings gave problems (standard procedure optimized for unirradiated chip): further investigation



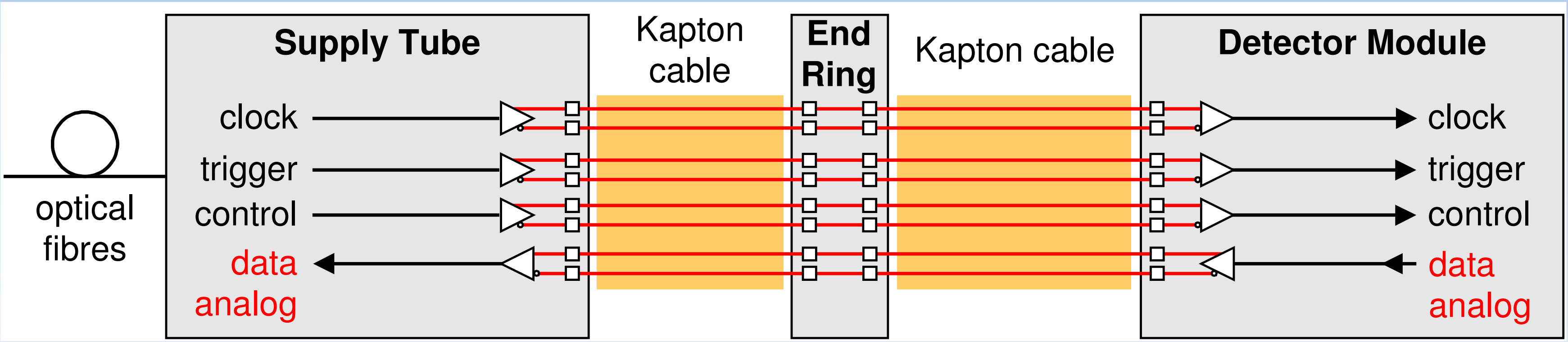
10000e- is still fine **but** operating with V_{dep} =450V

→ no benefit charge sharing (single pixel clusters)

→ degradation in spatial resolution

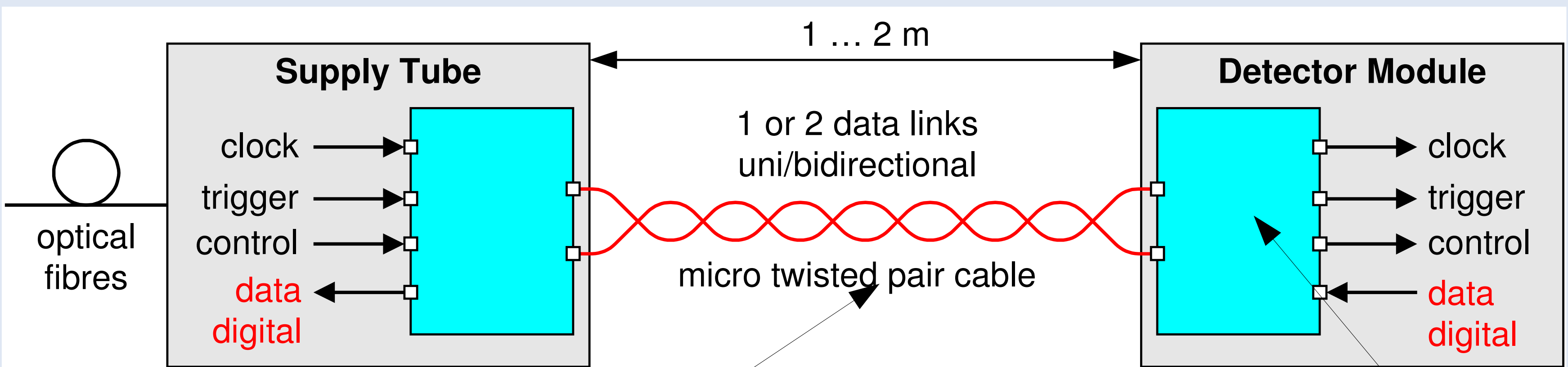
Idea for saving the material budget at high eta

Existing System in CMS Pixel Detector



New Concept

Beat Meier, PSI. TWEPP Conference September 2008



(I) Study the electrical cable properties

(II) Expand the squared blocks

Idea for saving the material budget at high eta

Optimize the comunication link between the detector and the optical system using a <u>long cable</u> for the transmission of analog/digital signals

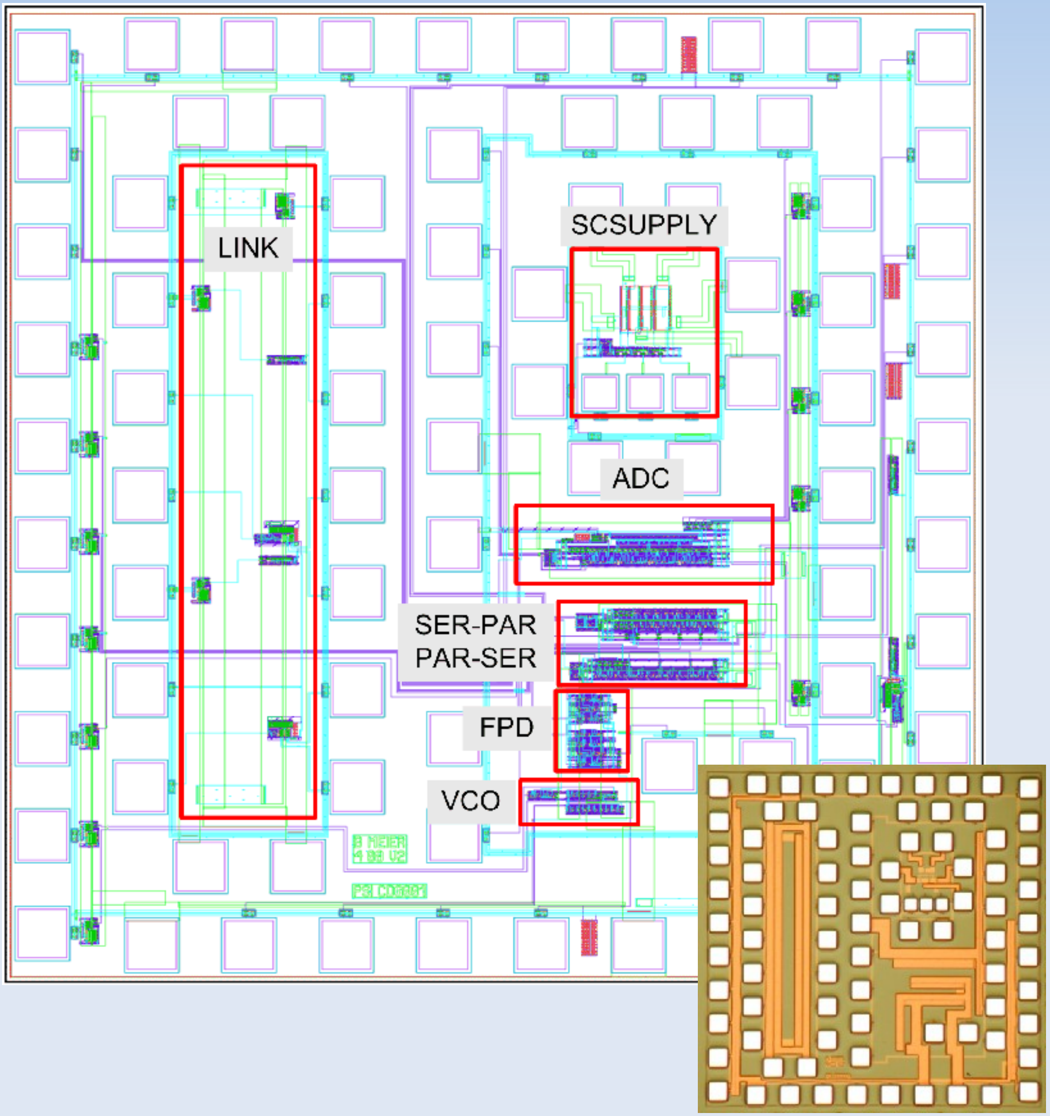
- AOHs, DOHs, Mother boards, PLL... further back
  - without impedance breaks (no end flange print)
  - remove kapton cable: expensive, length < 40cm, can only bend one plane

Further Requirements:

- minimal material budget → micro twisted pair (unshielded)
- minimal power consumption and noise → differential signal
- Minimal number of cables → serial data link
- 160 or 320 Mbit/s (4x or 8x LHC clock)
- Up to 2 m cable length

Soulution: (B.Meier and R. Horisberger):
µ -twisted pair cable of d=125µ m of Copper Cladded Aluminum (CCA). Ordered 9Km from **Elektrisola (CH).**

Test Chip layout



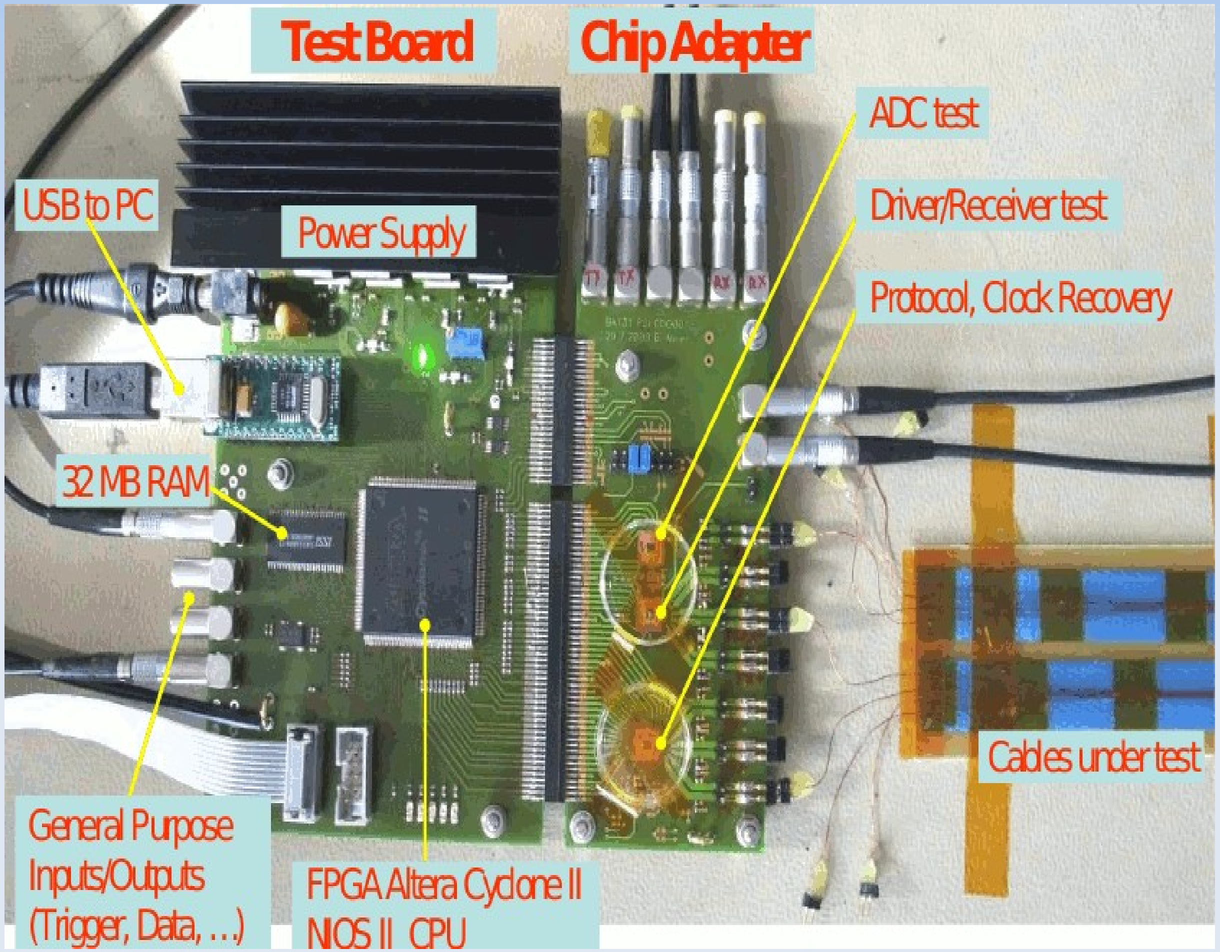
Design of a first test chip
(by B. Meier and PSI Chip Design Core Team)

- Size: 2 x 2 mm
- Technology: 250 nm CMOS IBM
- radiation hardness design
- design time was 4 weeks
  CERN MPW submitted in April 2008
  - Delivered end of July

- Basic components implemented:

Differential drivers
Differential receivers
PLL
ADC

Test System



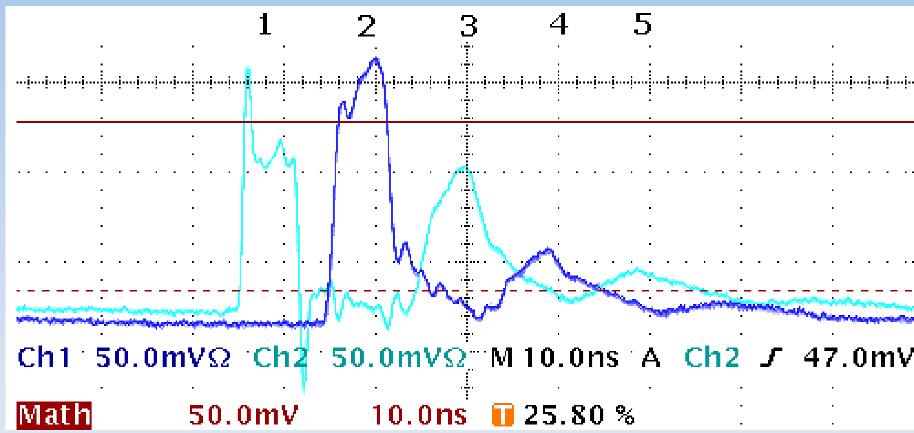
Beat Meier, PSI TWEPP Conference September 2008

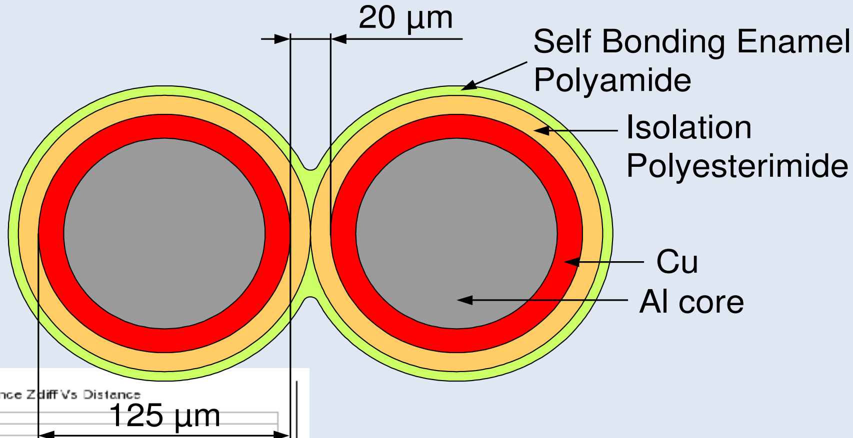
R&D plan:

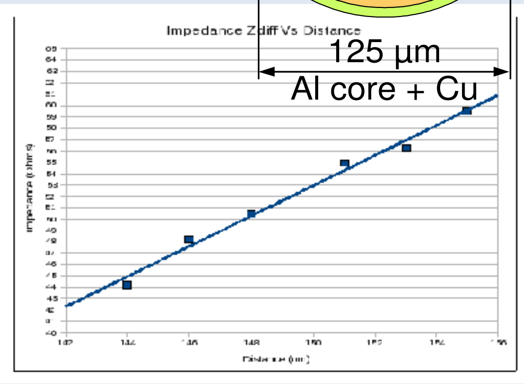
(I) Cable characterization:
- impedence
- signal loss
- signal quality
- bir error reate
- cross talk
- high frequency transmission

(II) New digital protocol implementation:
- test PLL clock recovery
- test PLL clock multiplier
- test of the ADC
- implement the protocol

Cable characterization







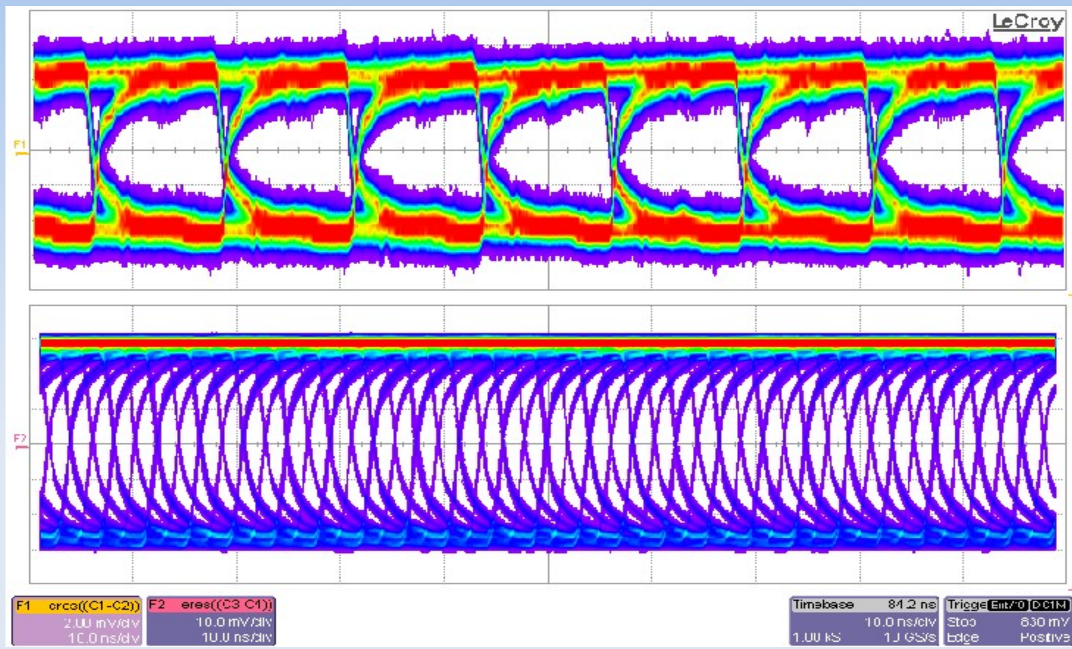
Impedance 29 ± 2 ohms
power loss 2m cable 50%

- ATLC simulation to determine the impedance variation vs the distance between the cables →
  1.3 Ohms per 1 µm distance variation

- SPICE simulation to determine the parasitic effects of the set up.

PIRE students at PSI and B.Meier

First results on 2m cable



Cross talk studies:

V_{diff} = 9 mV @ 80 Mbit/s

parallel line signal (asynchronous)

V_{diff} = 56 mV

Beat Meier

Very encouraging results:

Small bit error rate @ low V_{diff}

No Crosstalk

bidirectional link is possible!

- Further measurements:
  - cross talk between parallel lines up to 16 lines
  - transmission test @ 320MHz
  - Test longer cable
  - Test μ-tw cable drive a pixel barrel module

Scenarios for the intermediate upgrade

	Option	Layer/Radii	Modules	Cooling	Pixel ROC	Readout	Power
as 2008	0	4, 7, 11cm	768	C_6F_{14}	PS46 as now	analog 40MHz	as now
	1	4, 7, 11cm	768	C_6F_{14}	2x buffers	analog 40MHz	as now
	2	4, 7, 11cm	768	CO_2	2x buffers	analog 40MHz	as now
	3	4, 7, 11cm	768	CO_2	2x buffers	analog 40MHz µ -tw-pairs	as now
	4	4, 7, 11cm	768	CO_2	2xbuffer, ADC 160MHz serial	digital 320MHz µ -tw-pairs	as now
	5	4, 7, 11, 16cm	1428	CO_2	2xbuffer, ADC 160MHz serial	digital 640 MHz µ -tw-pairs	DC-DC new PS

- (R. Horisberger, SLHC meeting at CERN 21/05/08)

Conclusions:

- We have to replace pixel for phase 1 using the existing services :
  - Option 0: No change:

    → inefficiency problem at 4cm
  - Option 1: Double the buffer size:

    → is possible with the present module mechanics

    → no R&D needed but careful verifications
  - Option 3: µ-tw-pair cable and Analog signal, 40MHz

    → no change in the TBM and the ROC

    → important reduction of the material budget
  - Option 4: µ-tw-pair cable and digital read out @ 320MHz

    → ROC and TBM modifications

    → New digital protocol implementation

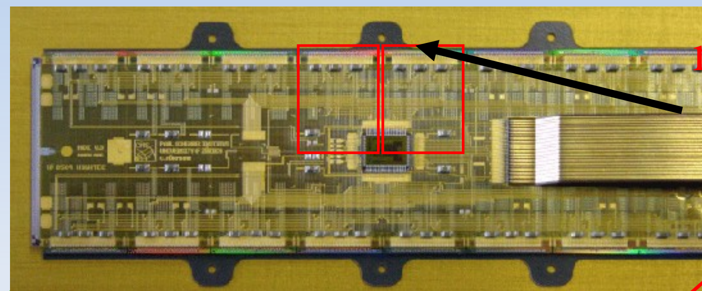
backup

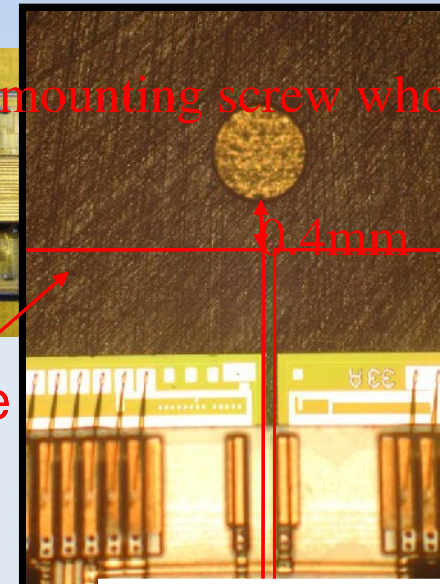
Data loss possible solutions

skip

Present system: 12 timestamp buffers, 32 data buffers

For 2013 upgrade: **Improve rate capability:**





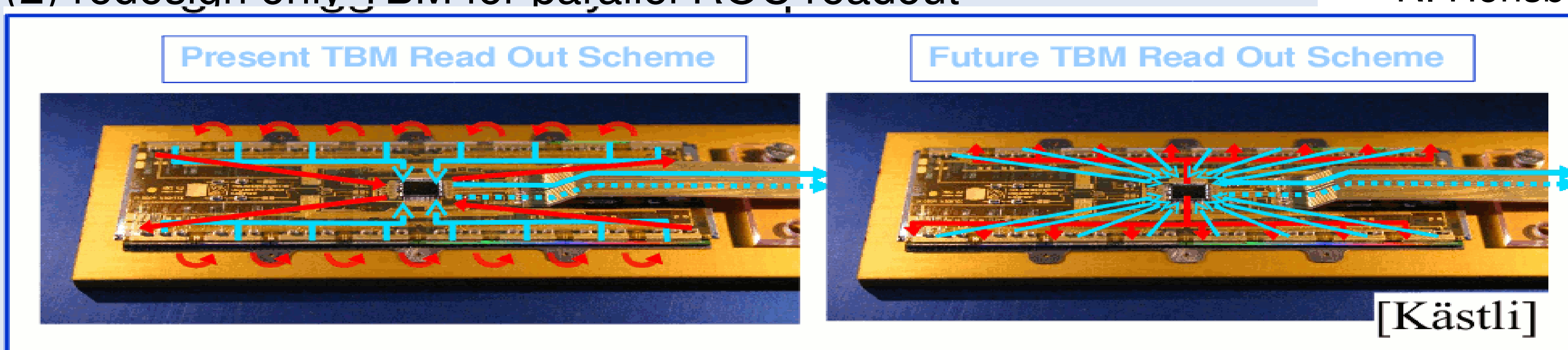
new ROC size

- R. Horisberger

(1) doubling the buffer size (24/64)

- 0.25mm technology just possible
- No R&D but carefully verification with high rate test beam

(2) redesign only TBM for parallel ROC readout



New module would be fully compatible with present system

Scenarios for the intermidiate upgrade

BPIX Option 0:

Replace the current pixel system with identical pixel modules.

Detector designed in 1997 for Luminosity of $1x10^{34}$ will develop substantial inefficiency for 4cm layer at $2x10^{34}$ → Data Loss

BPIX Option 1:

Same Option 0 and Double the read out buffer size.

Current material budget is acceptable in eta region 0 but could be improved, especially in eta region 1.4-2.3

BPIX Option 3 or 4:

CO_2 cooling,
high speed link with µtw pairs cable